Electronic Version

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Claims

[c1] A method of fabricating a gate electrode for a semiconductor comprising the steps of: providing a substrate; providing on the substrate a layer of a first material of thickness t_p, the first material being selected from the group consisting of Si, Si_{1-x}-Ge_x alloy, Ge and mixtures thereof and a layer of metal of thickness t_m; and annealing the layers, such that substantially all of the first material and the metal are consumed during reaction with one another.

[c2] The method of claim 1 wherein the metal is selected from one of the group consisting of Ni, Pd, Pt, Co, Ti and alloys of these materials including Ni-Pt, Ni-Pd, Ni-Co.

[c3] The method of claim 1 wherein the first material layer is applied to the substrate and the metal layer is provided on the first material layer.

[c4] The method of claim 1 wherein the thicknesses t_p and t_m are related by a predetermined ratio of t_m/t_p.

[c5] The method of claim 4 wherein the ratio of t_m/t_p is determined by the particular first material and metal to be annealed.

[c6] The method of claim 1 wherein annealing is performed at temperatures ranging from 300 to 900°C.

[c7] The method of claim 1 further comprising the step of depositing a further layer of metal on the gate electrode to increase gate thickness.

[c8] The method of claim 7 comprising forming source/drain contacts simultaneously with the gate electrode.

[c9] The method of claim 8 wherein as much as 5% of one of the first material and the metal remains following reaction with the other of the metal and the first material.

[c10] The gate electrode for a semiconductor device comprising a substrate and a gate layer thereon formed by the annealing of a first material with a metal, substantially all of the first material and the metal having been consumed during reaction with one another, the resultant layer comprising the gate electrode.

[c11] The gate electrode of claim 10, wherein the metal is selected from one of the group consisting of Ni, Pd, Pt, Co, Ti and alloys of these materials including Ni-Pt, Ni-Pd, Ni-Co.

[c12] The gate electrode of claim 10, wherein the first material is selected from the group consisting of Si, $Si_{1-x}Ge_x$ al-

loy, Ge and mixtures thereof.

[c13] The gate electrode of claim 10 wherein as much as 5% of one of the first material and the metal remains following reaction with the other of the metal and the first material.

[c14] The gate electrode of claim 13, wherein a layer of metal is provided on the gate layer.

[c15] The gate electrode of claim 10 wherein the gate electrode is incorporated in a CMOS semiconductor device.

[c16] A method for forming an integrated circuit comprising:
providing a substrate;
depositing an amorphous polycrystalline first layer on the substrate, the first layer comprising a material having a work function close to the mid-gap of silicon band gap;
patterning the first layer to form a gate electrode of a transistor and forming first and second diffusion regions of the transistor; and
wherein the material of the first layer reduces problems associated with inversion and agglomeration associated with formation of the transistor.

[c17] The method of claim 16 wherein:
patterning the first layer comprises forming gate elec-

trodes of at least a first PMOS transistor and a first NMOS transistor to form a CMOS integrated circuit; and
the material of the first layer comprises silicon, germanium, alloys or a combination thereof, including $Si_{1-x}Ge_x$.

[c18] The method of claim 16 wherein the material of the first layer comprises silicon, germanium, alloys or a combination thereof, including $Si_{1-x}Ge_x$.

[c19] The method of claim 16 further comprises:
depositing a metal layer over the substrate after the gate electrode and diffusion regions of the transistor are formed; and
processing the metal layer to cause a reaction between the material of the first layer and metal layer such that substantially all the material of the first layer and portion of the metal layer over the first layer are consumed.

[c20] The method of claim 19 wherein processing the metal layer comprises annealing or rapid thermal annealing.

[c21] The method of claim 20 wherein unconsumed first layer is less than or equal to 5% and unreacted metal layer is less than or equal to 10%.

[c22] The method of claim 19 wherein the processing the metal layer also forms silicide over the diffusion regions.

[c23] The method of claim 22 wherein processing the metal layer comprises annealing or rapid thermal annealing.

[c24] The method of claim 23 wherein unconsumed first layer is less than or equal to 5% and unreacted metal layer is less than or equal to 10%.

[c25] The method of claim 19 wherein a metal material of the metal layer comprises Ni, Pd, Pt, Co, Ti, or a combination or alloys thereof including Ni-Pt, Ni-Pd, and Ni-Co.

[c26] The method of claim 25 wherein the processing the metal layer also forms silicide over the diffusion regions.

[c27] The method of claim 26 wherein processing the metal layer comprises annealing or rapid thermal annealing.

[c28] The method of claim 25 wherein processing the metal layer comprises annealing or rapid thermal annealing.

[c29] The method of claim 19 wherein the first layer comprises a first thinkness t_p and the metal layer comprises a second thickness t_m, and wherein a minimum of a ratio of the first and second thickness t_p/t_m results in consumption or substantially the first and metal layers during processing of the metal layer.

[c30] The method of claim 29 wherein processing the metal

layer comprises annealing.

[c31] The method of claim 29 wherein the processing the metal layer also forms silicide over the diffusion regions.

[c32] The method of claim 31 wherein processing the metal layer comprises annealing or rapid thermal annealing.

[c33] The method of claim 19 further comprises etching remaining portion of unreacted metal layer above the gate electrode after processing the metal layer.

[c34] The method of claim 33 wherein processing the metal layer comprises annealing.

[c35] The method of claim 34 wherein the processing the metal layer also forms silicide over the diffusion regions.

[c36] The method of claim 35 wherein processing the metal layer comprises annealing or rapid thermal annealing.

[c37] The method of claim 19 wherein the first layer comprises a first thinkness t_p and the metal layer comprises a second thickness t_m, and wherein a minimum of a ratio of the first and second thickness t_p/t_m results in consumption or substantially the first and metal layers during processing of the metal layer.

[c38] The method of claim 37 wherein processing the metal

layer comprises annealing.

[c39] The method of claim 37 wherein the processing the metal layer also forms silicide over the diffusion regions.

[c40] The method of claim 39 wherein processing the metal layer comprises annealing or rapid thermal annealing.

[c41] An integrated circuit comprising a transistor having a gate electrode and first and second diffusion regions wherein the gate electrode is formed from an amorphous polycrystalline first layer comprising a material having a work function close to the mid-gap of silicon band gap, the material reduces problems associated with inversion and agglomeration associated with formation of the transistor.